Integrated Plasma Control in Next-Generation Devices Using DIII–D Modeling and Simulation Approaches[*]

R.D. Deranian,[1] J.A. Leuer,[1] J.R. Ferron,[1] D.A. Humphreys,[1] R.D. Johnson,[1] B.G. Penaflor,[1]
M.L. Walker,[1] A.S. Welander,[1] B. Wan,[2] Y. Gribov,[3] M. Kwon,[4] H. Jhang,[4]
and R.R. Khayrutdinov[5]

[1]*General Atomics, P.O. Box 85608, San Diego, California 92186-5608*
e-mail: deranian@fusion.gat.com
[2]*Academia Sinica, IPP, P.O. Box 1126, Hefei 230031, Anhui Province China*
[3]*ITER Naka, 801-1 Mukouyama, Naka-machi, Naka-gun, Ibaraki-ken, 31-0193*
[4]*Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea*
[5]*TRINITI Laboratory, Troitsk, Moscow, Russia*

An extensive set of software tools for integrated plasma control has been developed, validated, and applied to the DIII–D tokamak to design controllers for plasma shape and both axisymmetric and non-axisymmetric MHD instabilities [1]. The integrated plasma control approach uses validated physics models to design controllers, and confirms their performance by operating actual machine control hardware and software against detailed tokamak system simulations. These tools are being applied to several fusion device designs which require integrated plasma control for high reliability advanced tokamak or burning plasma operation, including KSTAR, EAST, and ITER. DIII–D physics-based models include conductors, diagnostics, power supplies, and both linear and nonlinear plasma models. Controller designs are based on multivariable linear methods and are robust to model uncertainty in dynamic shaping performance. Simulations incorporating detailed models are performed offline to confirm performance in the presence of such nonlinear effects as voltage saturation, power supply rate limits, and plasma configuration changes (e.g. from single to double-null). Plasma control systems (PCS) based on the DIII–D PCS [2] have been designed for each of these devices. These systems can be connected to the detailed control simulations to verify event handling and demonstrate functioning of control action under realistic hardware (cpu and network) conditions. Results of simulations are shown, illustrating limitations on performance imposed by each device design, engineering choices, and control system algorithms and hardware. Such simulations allow confirmation of performance prior to actual implementation on an operating device.

[1]   D.A. Humphreys, Proc. 20th IEEE/NPSS, San Diego, CA (2003).
[2]   B.G. Penaflor, Proc. 4th IAEA Tech. Mtg. on Ctrl Data Acq., San Diego, CA (2003).